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METHOD FOR PRODUCING AN ANTIFUSE IN A SUBSTRATE AND AN ANTIFUSE STRUCTURE FOR INTEGRATION IN A SUBSTRATE

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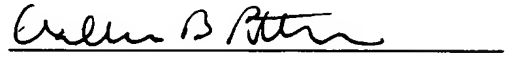
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METHOD FOR PRODUCING AN ANTIFUSE IN A SUBSTRATE AND AN ANTIFUSE STRUCTURE FOR INTEGRATION IN A SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority benefits under 35 U.S.C. §119 to co-pending German patent application 102 55 427.7-33, filed November 28, 2002. This related patent application is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The invention relates to a method for producing an antifuse in a substrate, in particular in an integrated circuit, and an antifuse structure for integration in an integrated circuit.

Description of the Related Art

[0003] Antifuse structures are used in integrated circuits to permanently store setting values. For this purpose, antifuse structures can be programmed by being changed over from a high-impedance to a low-impedance state by means of an applied programming voltage. The high-impedance and low-impedance states are permanent, i.e., they are maintained permanently without the presence of a voltage. In this way, the antifuse structure can serve as a binary storage element, the two states being determined by the high-impedance state and the low-impedance state.

[0004] Antifuse structures usually have a first conductive region and a second conductive region isolated from one another by a dielectric. The dielectric forms a thin layer between the first conductive region and the second conductive region, which layer is initially nonconductive, or at high impedance. When a programming voltage is applied, an electric field forms between the two conductive regions, a breakdown channel forming at that location in the dielectric at which the breakdown field strength of the dielectric is exceeded by the electric field, which breakdown

channel permanently alters the dielectric in such a way that a low-impedance channel is formed.

[0005] Conventional antifuse structures are usually produced by stacking layers one on top of the other, the method steps of deposition of a first conductive layer, patterning of the first conductive layer, deposition of a dielectric layer, patterning of the dielectric layer and deposition of a second conductive layer and patterning of the second conductive layer essentially being carried out one after the other.

[0006] In order to deposit said layers one above the other, relatively large overlay tolerances are necessary, with the result that when the feature sizes of the integrated circuit are miniaturized, the layers of the antifuse structure cannot be miniaturized to the same extent.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide a method for producing an antifuse structure in a substrate and an antifuse structure, free scalability of the antifuse structure being afforded.

[0008] A first aspect of the present invention provides a method for producing an antifuse in a substrate. For this purpose, a first interconnect is applied to the substrate, a dielectric layer being applied at an end face of the first interconnect, which end face essentially runs vertically with respect to the substrate. A second interconnect is subsequently applied to the substrate in such a way that it adjoins the dielectric layer with an end face, with the result that an antifuse structure is formed.

[0009] The production method according to the invention for an antifuse has the advantage that it is possible to avoid overlay tolerances in the mask process and negative effects such as, e.g., "void" formation in the case of the metal fill. As a result, free scalability is possible in the case of the invention's method for producing

the antifuse. It may be provided that the dielectric layer is applied isotropically, with the result that edges of the first interconnect are covered. The possibility of short circuits with respect to the edges of the first interconnect arising during the application of the second interconnect is avoided in this way.

[0010] It may be provided that the dielectric layer is applied with the aid of an anisotropic deposition process by carrying out the deposition process obliquely with respect to the surface of the substrate. Consequently, the dielectric layer can be applied on the end face in a simple manner, improved edge coverage also being ensured by the direction of the deposition process obliquely with respect to the surface.

[0011] It may be provided that the first interconnect is applied in such a way that it terminates with a surface of the substrate. This may preferably be carried out in such a way that the first interconnect is introduced into a trench structure in the substrate and the surfaces of the first interconnect and of the substrate are subsequently processed in such a way that they terminate with one another in a common surface. In order to form an antifuse structure, the second interconnect is preferably introduced into a second trench structure in the substrate, the second trench structure being arranged in such a way that the second interconnect introduced therein is connected to the dielectric layer by its end face.

[0012] In this way, it is possible to produce an antifuse structure which is introduced in a continuous interconnect formed from the first interconnect and the second interconnect, so that the antifuse structure thus formed takes up only a small area. Furthermore, the process is self-aligning since the dielectric layer can be produced without a mask step.

[0013] It may be provided that, for the purpose of introducing the conductor material for the first interconnect into the first trench structure, firstly a sacrificial material is introduced into the second trench structure, the conductor material for the first

interconnect being applied over the area. The conductor material is subsequently removed above the second trench structure by removing the sacrificial material. As an alternative, it is also possible to remove the conductor material by means of a CMP process, the conductor material essentially being completely removed everywhere except in the first trench structure, so that only the conductor material in the first trench structure and the sacrificial material in the second trench structure remain. Afterward, in order to introduce the dielectric layer and the second interconnect, the sacrificial material may be removed and the dielectric layer and the second interconnect may be introduced.

[0014] A further aspect of the present invention provides an antifuse structure in a substrate with a dielectric layer between a first interconnect and a second interconnect. The dielectric layer is essentially arranged vertically with respect to the surface of the substrate and arranged between end faces of the first and second interconnects.

[0015] In this way, it is possible to produce an antifuse structure which is essentially freely scaleable and needs a smaller area requirement than conventional antifuse structures.

[0016] It may be provided that the first interconnect, the dielectric layer and the second interconnect are arranged in a trench structure in a substrate. The trench structure has the advantage in the production method that the processes are self-aligning, so that, e.g., the production of the dielectric layer does not require a further mask process.

[0017] It may be provided that the first interconnect, the dielectric layer and the second interconnect are arranged in the substrate in such a way that their surfaces terminate with the surface of the substrate. In this way, it is possible to produce a surface on which further layers can be applied, e.g., in order to form further metallization layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Preferred embodiments of the invention are explained in more detail below with reference to the accompanying drawings, in which:

[0019] Figures 1a to 1c show the individual method steps according to the invention in accordance with a first embodiment of the invention; and

[0020] Figure 2 shows a cross section through an antifuse structure according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0021] Figures 1a to 1c illustrate, in accordance with a first embodiment of the invention, the method steps for producing an antifuse structure in a substrate 1. A trench structure 2 is introduced into the substrate, which trench structure is intended to accommodate the later interconnect and the antifuse structure.

[0022] The trench structure 2 is preferably arranged in an ILD region (Inter Layer Dielectric). After the deposition of the first metal layer and the subsequent CMP process, the conductor material is removed from the second part of the trench structure with the aid of an RIE method.

[0023] A first interconnect 3 is then introduced into a first part of the trench structure 2, which interconnect ends in the trench structure 2 at the position of the later antifuse structure and has an end face 4. The first interconnect 3 can be introduced in various ways. By way of example, it is possible to apply a layer with conductive material over the trench structure 2, which layer is deposited over the area, that is to say both on the substrate surface 1 and in the trench structure 2. Afterward, by means of masking, the layer with conductive material can be removed in such a way that only the first interconnect 3 remains and the conductive material situated on the

substrate surface 1 and in a second part of the trench structure 2 is removed. The conductive material is preferably a metallic material, and may comprise, by way of example, aluminum, copper, tungsten and/or other conductor materials known in semiconductor technology.

[0024] The end face 4 preferably runs vertically with respect to the substrate surface, but may also run obliquely with respect to the substrate surface, depending on the production process. Running obliquely has the advantage that the area between the conductor and the dielectric can be enlarged, so that a high breakdown probability can be achieved during the later "blowing" of the antifuse and it is thus possible to improve the overall yield of an integrated circuit with such antifuse structures. In particular, from a process engineering standpoint, angles of between 0° and 60° between the normal to the surface and the end face are advantageous since these can be achieved in a simple manner by tilting the substrate wafer during a lithography step.

[0025] Figure 1b illustrates that a dielectric layer 5 is applied to the structure thus obtained. The dielectric layer 5 must be applied in such a way that the end face 4 is completely covered in a defined manner. In particular, the edges of the end face 4 should be covered in order to avoid a short circuit between the first interconnect and a second interconnect 6 that is subsequently to be applied.

[0026] In order to achieve this, an isotropic deposition process is preferably used for depositing the dielectric layer 5. When using an anisotropic deposition process, it is preferably to be provided that the material to be deposited is applied obliquely to the substrate surface, so that the angle of application to the end face 4 becomes as large as possible, and is as far as possible 90° in the optimum case. This is possible in a particularly simple manner if the end face runs oblique with respect to the surface.

[0027] The dielectric layer 5 is nonconductive and may essentially comprise all dielectric materials known in semiconductor technology. Silicon nitrite may preferably be used as the dielectric.

[0028] Since the dielectric layer 5 is very thin, e.g., 3 nm, in comparison with the order of magnitude of the trench structure 2, the dielectric layer 5 may remain in the trench structure when the second interconnect is introduced into the second part of the trench structure 2, and serves as additional insulation of the second interconnect from the substrate 1, as a result of which leakage currents can be reduced. Therefore, the location of the antifuse structure should preferably be chosen in such a way that the length of the interconnect is essentially formed by the second interconnect and the first interconnect is kept as short as possible.

[0029] The introduction of the second interconnect 6 is effected in the same way as the introduction of the first interconnect by deposition of a conductor material and subsequent removal of the conductor material from the substrate surface. The removal of excess conductor material from the substrate surface may be carried out by means of a CMP method.

[0030] This results in an antifuse structure in which the dielectric layer 5 is essentially arranged vertically or obliquely with respect to the interconnect. The antifuse structure which has been produced by the method according to the invention has the advantage that it is essentially freely scaleable and that it forms an essentially planar surface with the substrate surface, so that further metal layers or other layers can be arranged thereabove.

[0031] It may be provided that, in addition to the dielectric layer 5, an electrode layer (not shown) made of a readily migrating material, e.g., WSi, is also deposited isotropically. The electrode layer made of readily migrating material improves the breakdown behavior and, during the blowing of the antifuse, ensures that the breakdown channel does not recede during the lifetime of the circuit.

[0032] It goes without saying that provision may also be made for arranging the antifuse structure according to this invention on the substrate surface rather than in a trench structure. The advantage of providing the antifuse structure in the trench structure 2 is that the processes are essentially self-aligning, in particular the process of depositing the dielectric layer 5.

[0033] Figure 2 shows a cross section along the interconnect of the antifuse structure, as illustrated in Figure 1c. It can be seen that the dielectric layer is essentially situated vertically in the interconnect in such a way that the two parts of the interconnect are not connected to one another, but rather are connected only via the dielectric layer 5.